

# **LAYOUT OF A FLASH MEMORY HAVING SYMMETRIC SELECT TRANSISTORS**

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## **ABSTRACT OF THE DISCLOSURE**

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A layout of flash memory having symmetric select transistors includes a memory cell array and a polysilicon gate. The polysilicon gate forms a plurality of select transistors in coordination with a plurality of pairs of sources/drains, so as to connect to the memory cell array. The polysilicon is perpendicularly extended toward a direction of the memory cell array, thereby overcoming a drawback as select transistors being unsymmetrical in a prior flash memory structure.